

# Undervoltage Sensing Circuit

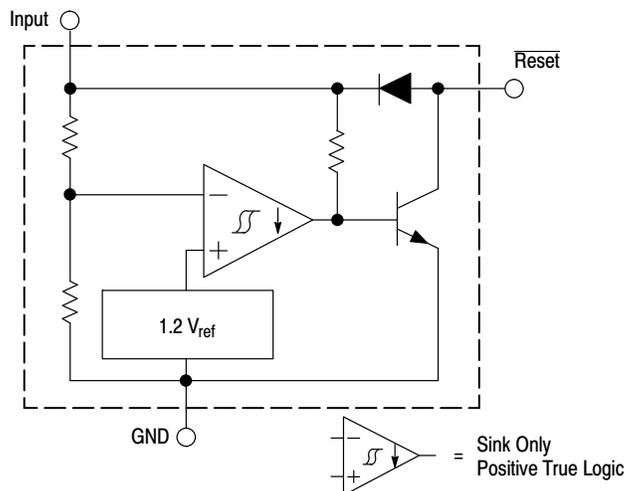
## MC34064, MC33064, NCV33064

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 V input with low standby current. The MC devices are packaged in 3-pin TO-92, micro size TSOP-5, 8-pin SOIC-8 and Micro8 surface mount packages. The NCV device is packaged in SOIC-8 and TO-92.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

### Features

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO-92, TSOP-5, SOIC-8 and Micro8 Surface Mount Packages
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These Devices are Pb-Free and are RoHS Compliant

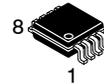


This device contains 21 active transistors.

Figure 1. Representative Block Diagram



SOIC-8  
D SUFFIX  
CASE 751



Micro8  
DM SUFFIX  
CASE 846A

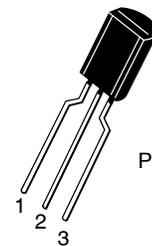


TSOP-5  
SN SUFFIX  
CASE 483

Pin 1. Ground  
2. Input  
3. Reset  
4. NC  
5. NC



STRAIGHT LEAD

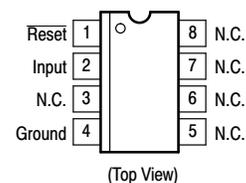


BENT LEAD

TO-92  
CASE 29-10

Pin: 1. Reset  
2. Input  
3. Ground

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

# MC34064, MC33064, NCV33064

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	$V_{in}$	-1.0 to 10	V
Reset Output Voltage	$V_O$	10	V
Reset Output Sink Current (Note 2)	$I_{Sink}$	Internally Limited	mA
Clamp Diode Forward Current, Reset to Input Pin (Note 2)	$I_F$	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	625	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	200	$^\circ\text{C/W}$
D Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	625	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	200	$^\circ\text{C/W}$
DM Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	520	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	240	$^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Operating Ambient Temperature	$T_A$		$^\circ\text{C}$
MC34064		0 to +70	
MC33064		-40 to +85	
NCV33064		-40 to +125	
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- ESD data available upon request.

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Notes 3 and 4] unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
<b>COMPARATOR</b>					
Threshold Voltage					V
High State Output ( $V_{in}$ Increasing)	$V_{IH}$	4.5	4.61	4.7	
Low State Output ( $V_{in}$ Decreasing)	$V_{IL}$	4.5	4.59	4.7	
Hysteresis	$V_H$	0.01	0.02	0.05	

## RESET OUTPUT

Output Sink Saturation	$V_{OL}$				V
( $V_{in} = 4.0\text{ V}$ , $I_{Sink} = 8.0\text{ mA}$ )		-	0.46	1.0	
( $V_{in} = 4.0\text{ V}$ , $I_{Sink} = 2.0\text{ mA}$ )		-	0.15	0.4	
( $V_{in} = 1.0\text{ V}$ , $I_{Sink} = 0.1\text{ mA}$ )		-	-	0.1	
Output Sink Current ( $V_{in}$ , $\overline{\text{Reset}} = 4.0\text{ V}$ )	$I_{Sink}$	10	27	60	mA
Output Off-State Leakage ( $V_{in}$ , $\overline{\text{Reset}} = 5.0\text{ V}$ )	$I_{OH}$	-	0.02	0.5	$\mu\text{A}$
Clamp Diode Forward Voltage, Reset to Input Pin ( $I_F = 10\text{ mA}$ )	$V_F$	0.6	0.9	1.2	V

## TOTAL DEVICE

Operating Input Voltage Range	$V_{in}$	1.0 to 6.5	-	-	V
Quiescent Input Current ( $V_{in} = 5.0\text{ V}$ )	$I_{in}$	-	390	500	$\mu\text{A}$

- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$  for MC34064                       $T_{high} = +70^\circ\text{C}$  for MC34064  
            $-40^\circ\text{C}$  for MC33064                       $+85^\circ\text{C}$  for MC33064  
            $-40^\circ\text{C}$  for NCV33064                     $+125^\circ\text{C}$  for NCV33064
- NCV prefix is for automotive and other applications requiring site and change control.

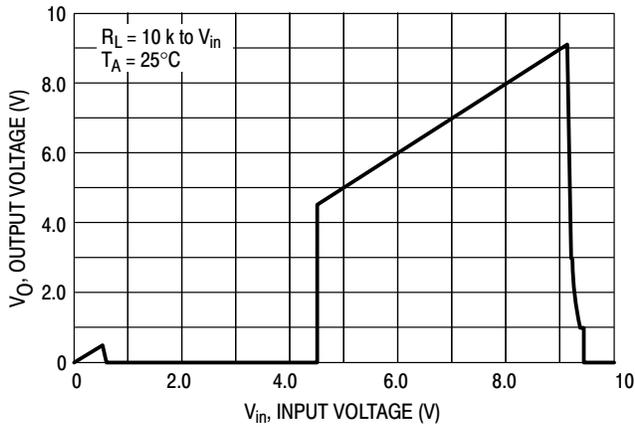


Figure 2. Reset Output Voltage versus Input Voltage

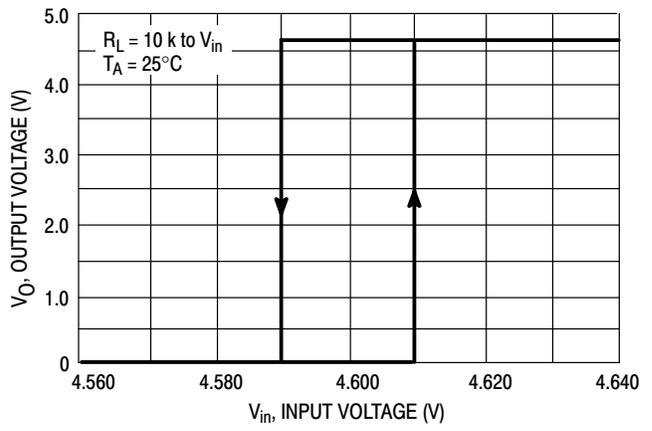


Figure 3. Reset Output Voltage versus Input Voltage

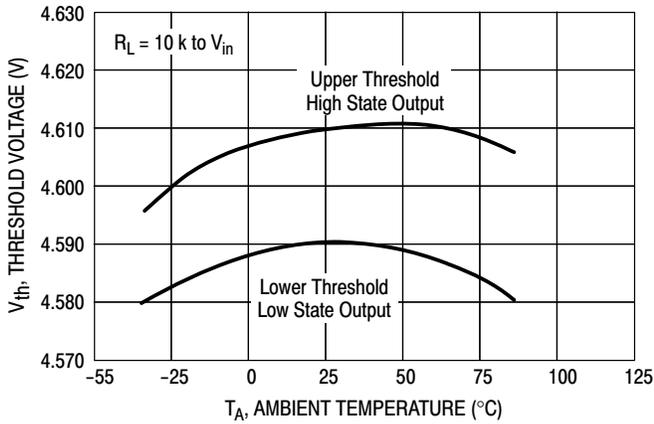


Figure 4. Comparator Threshold Voltage versus Temperature

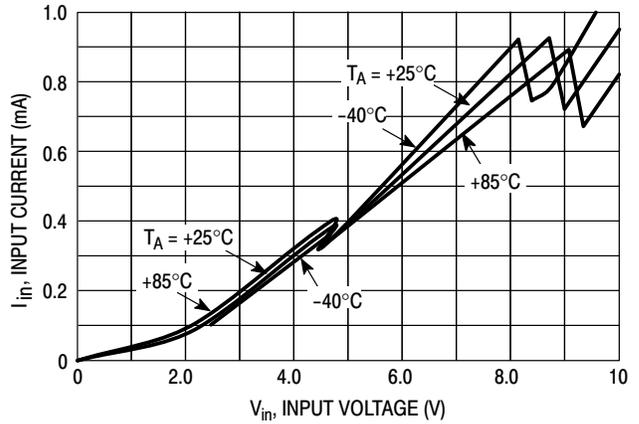


Figure 5. Input Current versus Input Voltage

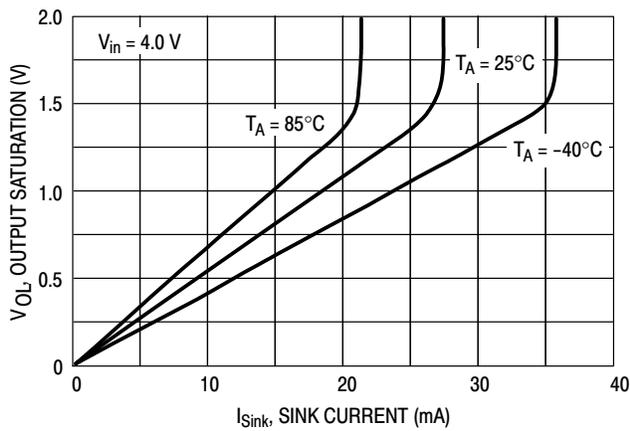


Figure 6. Reset Output Saturation versus Sink Current

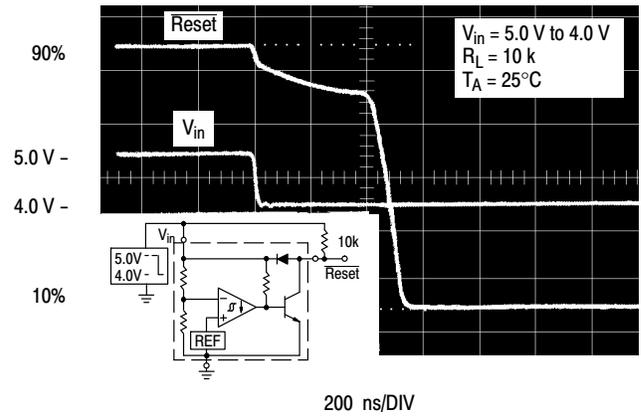


Figure 7. Reset Delay Time

# MC34064, MC33064, NCV33064

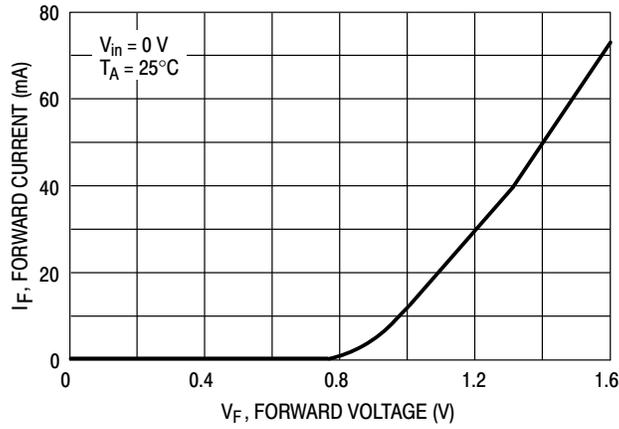


Figure 8. Clamp Diode Forward Current versus Voltage

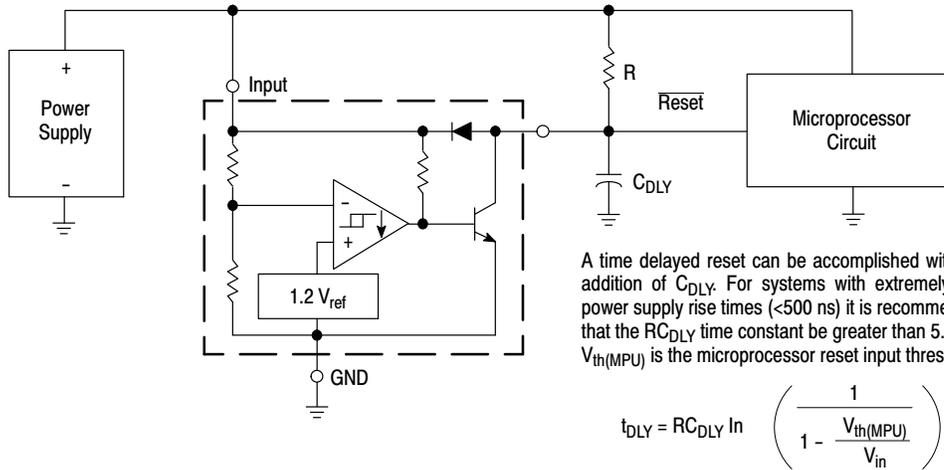
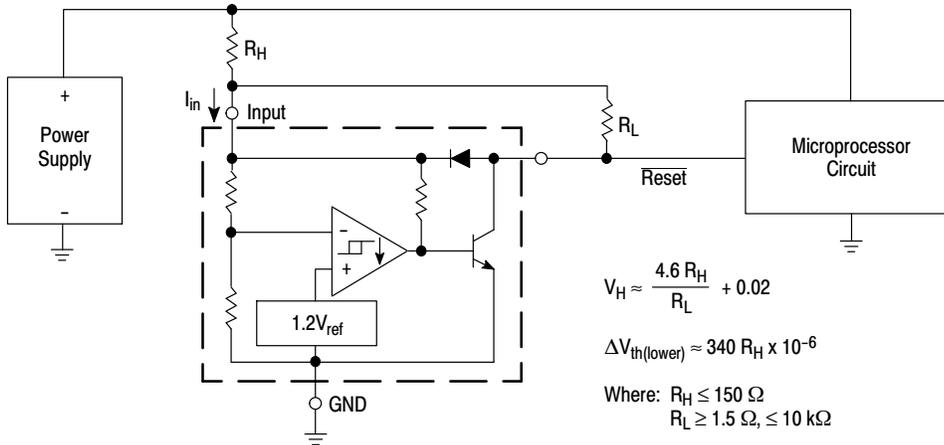


Figure 9. Low Voltage Microprocessor Reset

## TEST DATA



$V_H$ (mV)	$\Delta V_{th}$ (mV)	$R_H$ ( $\Omega$ )	$R_L$ (k $\Omega$ )
20	0	0	0
51	3.4	10	1.5
40	6.8	20	4.7
81	6.8	20	1.5
71	10	30	2.7
112	10	30	1.5
100	16	47	2.7
164	16	47	1.5
190	34	100	2.7
327	34	100	1.5
276	51	150	2.7
480	51	150	1.5

Comparator hysteresis can be increased with the addition of resistor  $R_H$ . The hysteresis equation has been simplified and does not account for the change of input current  $I_{in}$  as  $V_{CC}$  crosses the comparator threshold (Figure 4). An increase of the lower threshold  $\Delta V_{th(lower)}$  will be observed due to  $I_{in}$  which is typically  $340 \mu A$  at  $4.59 V$ . The equations are accurate to  $\pm 10\%$  with  $R_H$  less than  $150 \Omega$  and  $R_L$  between  $1.5 k\Omega$  and  $10 k\Omega$ .

Figure 10. Low Voltage Microprocessor Reset with Additional Hysteresis

# MC34064, MC33064, NCV33064

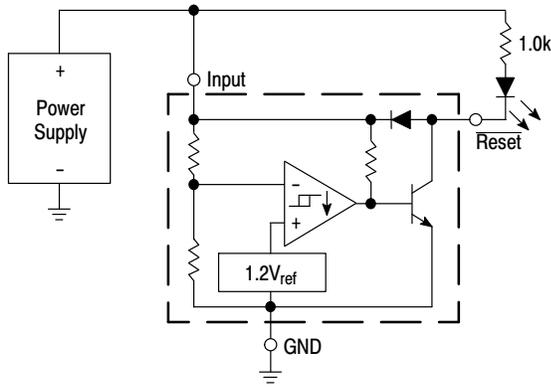


Figure 11. Voltage Monitor

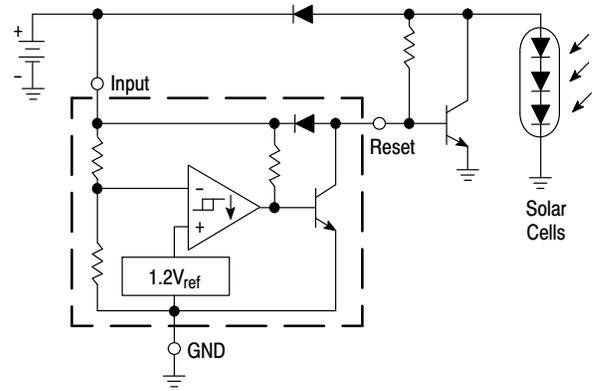
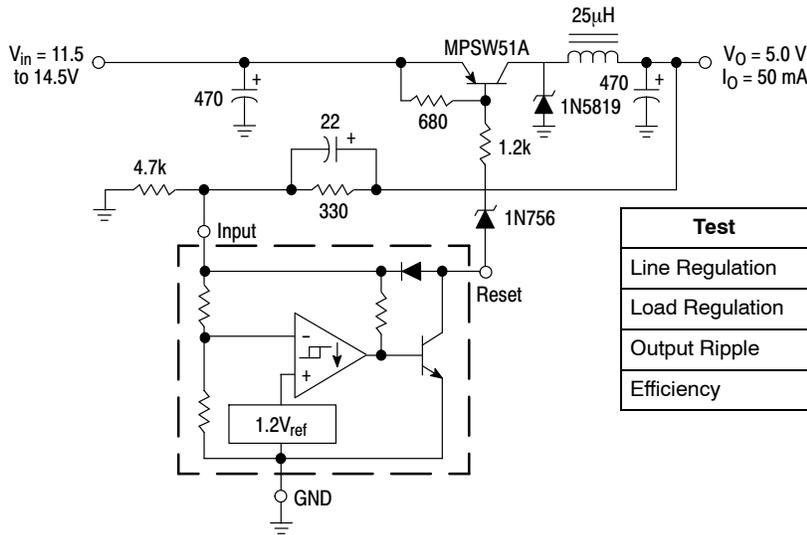
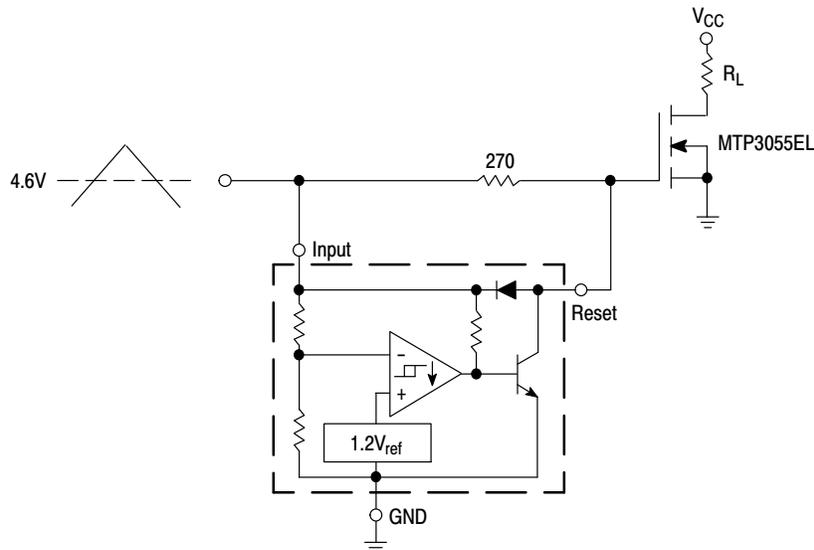


Figure 12. Solar Powered Battery Charger



Test	Conditions	Results
Line Regulation	$V_{in} = 11.5 \text{ V to } 14.5 \text{ V}, I_O = 50 \text{ mA}$	35 mV
Load Regulation	$V_{in} = 12.6 \text{ V}, I_O = 0 \text{ mA to } 50 \text{ mA}$	12 mV
Output Ripple	$V_{in} = 12.6 \text{ V}, I_O = 50 \text{ mA}$	60 mVpp
Efficiency	$V_{in} = 12.6 \text{ V}, I_O = 50 \text{ mA}$	77%

Figure 13. Low Power Switching Regulator



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC34064, its output grounds the gate of the L<sup>2</sup> MOSFET.

Figure 14. MOSFET Low Voltage Gate Drive Protection

# MC34064, MC33064, NCV33064

## ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping <sup>†</sup>
MC34064D-5G	T <sub>A</sub> = 0°C to +70°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC34064D-5R2G		SOIC-8 (Pb-Free)	2500 Units/ Tape & Reel
MC34064DM-5R2G		Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC34064P-5G		TO-92 (Pb-Free)	2000 Units / Bag
MC34064P-5RAG		TO-92 (Pb-Free)	2000 Units / Tape & Reel
MC34064P-5RPG		TO-92 (Pb-Free)	2000 Units / Ammo Pack
MC34064P-5RMG		TO-92 (Pb-Free)	
MC34064SN-5T1G		TSOP-5 (Pb-Free)	3000 Units / Tape & Reel
MC33064D-5G	T <sub>A</sub> = -40°C to +85°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC33064D-5R2G		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC33064DM-5R2G		Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC33064P-5G		TO-92 (Pb-Free)	2000 Units / Bag
MC33064P-5RAG		TO-92 (Pb-Free)	2000 Units / Tape & Reel
MC33064P-5RPG		TO-92 (Pb-Free)	2000 Units / Ammo Pack
MC33064SN-5T1G		TSOP-5 (Pb-Free)	3000 Units / Tape & Reel
NCV33064D-5R2G*	T <sub>A</sub> = -40°C to +125°C	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
NCV33064P-5RAG*		TO-92 (Pb-Free)	2000 Units / Tape & Reel
NCV33064P-5RPG*		TO-92 (Pb-Free)	2000 Units / Ammo Pack
NCV33064DM-5R2G*		Micro8 (Pb-Free)	4000 Units / Tape & Reel

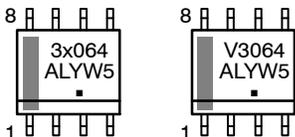
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV33064: T<sub>low</sub> = -40°C, T<sub>high</sub> = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

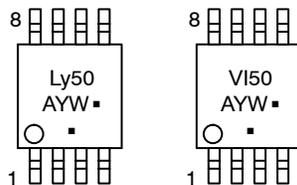
# MC34064, MC33064, NCV33064

## MARKING DIAGRAMS

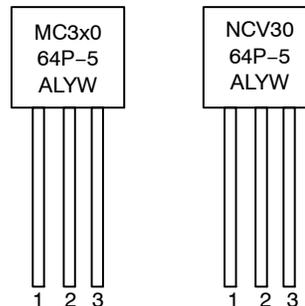
**SOIC-8**  
D SUFFIX  
CASE 751



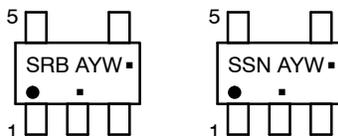
**Micro8**  
DM SUFFIX  
CASE 846A



**TO-92**  
P SUFFIX  
CASE 029



**TSOP-5**  
SN SUFFIX  
CASE 483



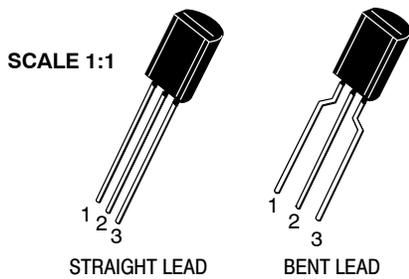
**MC34064**

**MC33064**

- x = 3 or 4
- y = C or I
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

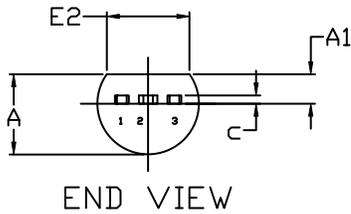
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**TO-92 (TO-226) 1 WATT**  
**CASE 29-10**  
**ISSUE D**

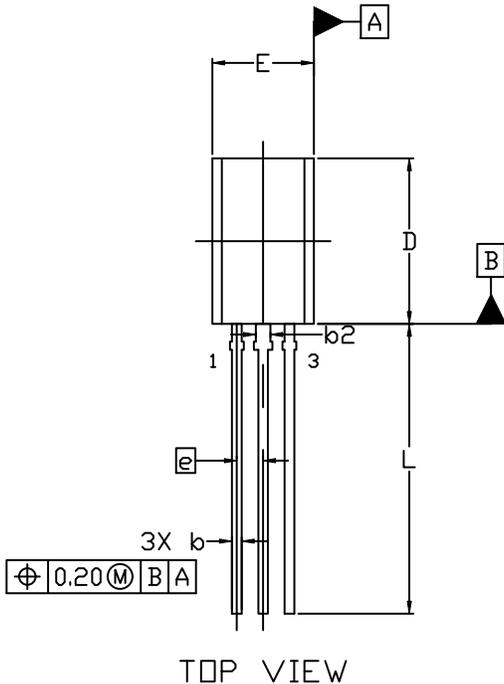
DATE 05 MAR 2021

**STRAIGHT LEAD**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

**STYLES AND MARKING ON PAGE 3**

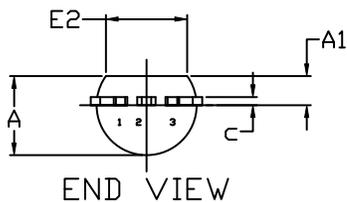
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<b>DESCRIPTION:</b>	<b>TO-92 (TO-226) 1 WATT</b>	<b>PAGE 1 OF 3</b>

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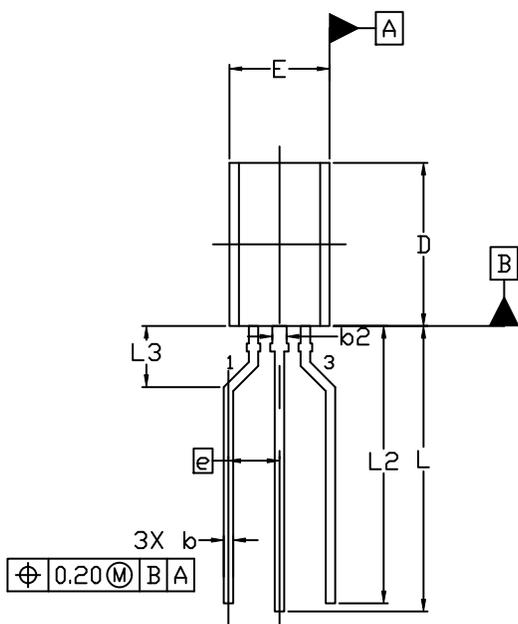
**TO-92 (TO-226) 1 WATT**  
**CASE 29-10**  
**ISSUE D**

DATE 05 MAR 2021

FORMED LEAD



END VIEW



TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
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b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

**STYLES AND MARKING ON PAGE 3**

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<b>DESCRIPTION:</b>	<b>TO-92 (TO-226) 1 WATT</b>	<b>PAGE 2 OF 3</b>

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**TO-92 (TO-226) 1 WATT  
CASE 29-10  
ISSUE D**

DATE 05 MAR 2021

- |   |  |  |   |   |
|---|--|--|---|---|
| <p>STYLE 1:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. COLLECTOR</p>             | <p>STYLE 2:<br/>PIN 1. BASE<br/>2. EMITTER<br/>3. COLLECTOR</p>                | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. ANODE<br/>3. CATHODE</p>               | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. CATHODE<br/>3. ANODE</p>            | <p>STYLE 5:<br/>PIN 1. DRAIN<br/>2. SOURCE<br/>3. GATE</p>            |
| <p>STYLE 6:<br/>PIN 1. GATE<br/>2. SOURCE &amp; SUBSTRATE<br/>3. DRAIN</p>  | <p>STYLE 7:<br/>PIN 1. SOURCE<br/>2. DRAIN<br/>3. GATE</p>                     | <p>STYLE 8:<br/>PIN 1. DRAIN<br/>2. GATE<br/>3. SOURCE &amp; SUBSTRATE</p> | <p>STYLE 9:<br/>PIN 1. BASE 1<br/>2. EMITTER<br/>3. BASE 2</p>            | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. GATE<br/>3. ANODE</p>          |
| <p>STYLE 11:<br/>PIN 1. ANODE<br/>2. CATHODE &amp; ANODE<br/>3. CATHODE</p> | <p>STYLE 12:<br/>PIN 1. MAIN TERMINAL 1<br/>2. GATE<br/>3. MAIN TERMINAL 2</p> | <p>STYLE 13:<br/>PIN 1. ANODE 1<br/>2. GATE<br/>3. CATHODE 2</p>           | <p>STYLE 14:<br/>PIN 1. EMITTER<br/>2. COLLECTOR<br/>3. BASE</p>          | <p>STYLE 15:<br/>PIN 1. ANODE 1<br/>2. CATHODE<br/>3. ANODE 2</p>     |
| <p>STYLE 16:<br/>PIN 1. ANODE<br/>2. GATE<br/>3. CATHODE</p>                | <p>STYLE 17:<br/>PIN 1. COLLECTOR<br/>2. BASE<br/>3. EMITTER</p>               | <p>STYLE 18:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. NOT CONNECTED</p>      | <p>STYLE 19:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE</p>              | <p>STYLE 20:<br/>PIN 1. NOT CONNECTED<br/>2. CATHODE<br/>3. ANODE</p> |
| <p>STYLE 21:<br/>PIN 1. COLLECTOR<br/>2. EMITTER<br/>3. BASE</p>            | <p>STYLE 22:<br/>PIN 1. SOURCE<br/>2. GATE<br/>3. DRAIN</p>                    | <p>STYLE 23:<br/>PIN 1. GATE<br/>2. SOURCE<br/>3. DRAIN</p>                | <p>STYLE 24:<br/>PIN 1. EMITTER<br/>2. COLLECTOR/ANODE<br/>3. CATHODE</p> | <p>STYLE 25:<br/>PIN 1. MT 1<br/>2. GATE<br/>3. MT 2</p>              |
| <p>STYLE 26:<br/>PIN 1. V<sub>CC</sub><br/>2. GROUND 2<br/>3. OUTPUT</p>    | <p>STYLE 27:<br/>PIN 1. MT<br/>2. SUBSTRATE<br/>3. MT</p>                      | <p>STYLE 28:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE</p>               | <p>STYLE 29:<br/>PIN 1. NOT CONNECTED<br/>2. ANODE<br/>3. CATHODE</p>     | <p>STYLE 30:<br/>PIN 1. DRAIN<br/>2. GATE<br/>3. SOURCE</p>           |
| <p>STYLE 31:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE</p>                 | <p>STYLE 32:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER</p>               | <p>STYLE 33:<br/>PIN 1. RETURN<br/>2. INPUT<br/>3. OUTPUT</p>              | <p>STYLE 34:<br/>PIN 1. INPUT<br/>2. GROUND<br/>3. LOGIC</p>              | <p>STYLE 35:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER</p>      |

**GENERIC  
MARKING DIAGRAM\***



- XXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98AON52857E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-92 (TO-226) 1 WATT</b>	<b>PAGE 3 OF 3</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

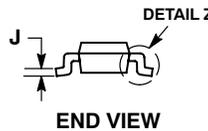
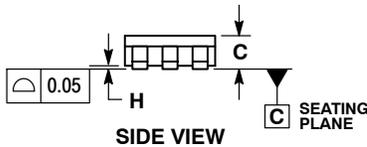
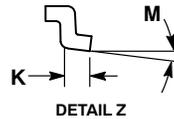
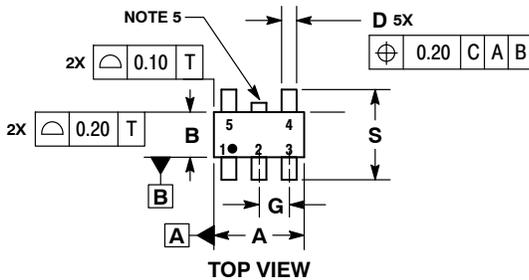
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SCALE 2:1

## TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

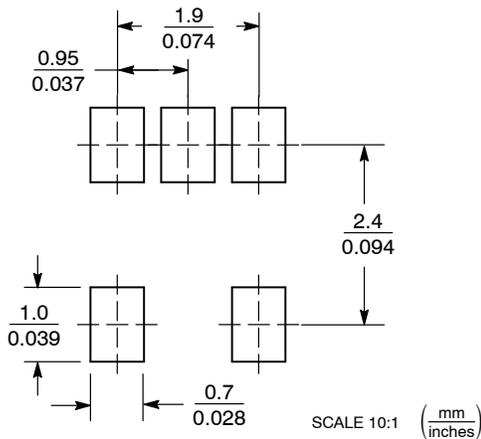


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

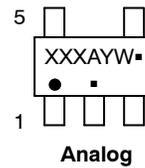
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*

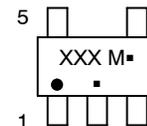


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

- |                            |                            |
|----------------------------|----------------------------|
| XXX = Specific Device Code | XXX = Specific Device Code |
| A = Assembly Location      | M = Date Code              |
| Y = Year                   | ▪ = Pb-Free Package        |
| W = Work Week              |                            |
| ▪ = Pb-Free Package        |                            |

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	TSOP-5	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

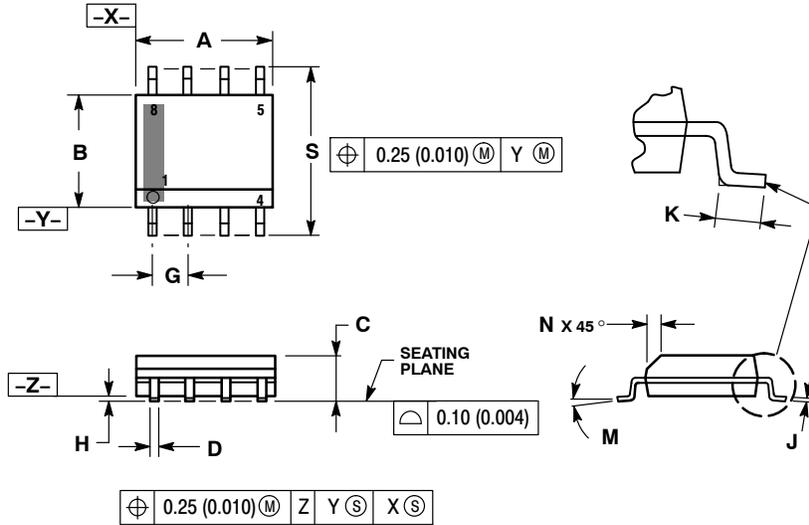
ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

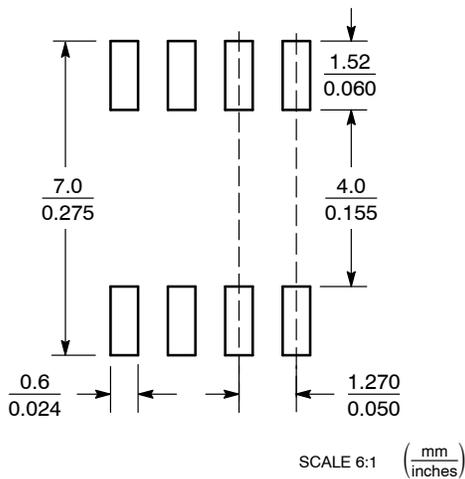
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

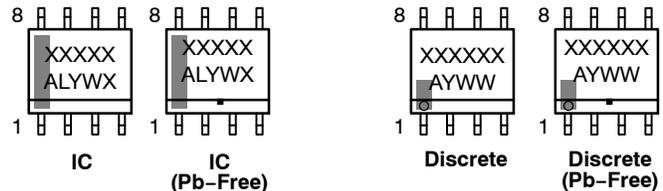
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

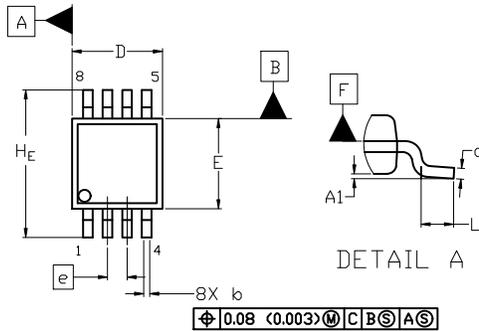
ON Semiconductor®



SCALE 2:1

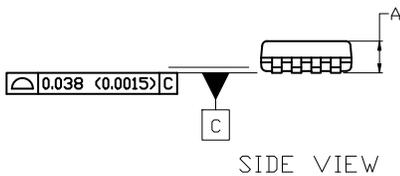
## Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020

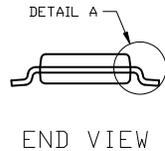


TOP VIEW

NOTE 3



SIDE VIEW



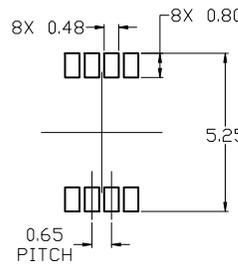
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀0.08 (0.003) M C B S A S

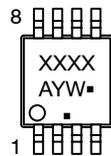
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H<sub>E</sub></i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED  
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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