ASUS® ASMM

System Monitoring Module

USER'S MANUAL

USER'S NOTICE

The product name and revision number are both printed on the product itself. Manual revisions are released for each product design represented by the digit before and after the period of the manual revision number. Manual updates are represented by the third digit in the manual revision number.

For previous or updated manuals, BIOS, drivers, or product release information, contact ASUS at http://www.asus.com.tw or through any of the means indicated on the following page.

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FCC & DOC COMPLIANCE

Federal Communications Commission Statement

This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

WARNING! The use of shielded cables for connection of the monitor to the graphics card is required to assure compliance with FCC regulations. Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

I. ASUS ASMM

Introduction

The ASUS ASMM (System Monitoring Module) allows you to monitor the system temperature, fan speed, and voltages to enhance system stability.

IMPORTANT! If your motherboard is equipped with the LM78 chipset, your system will report a warning since both LM78s (motherboard and ASMM's) use the same I/O address (0x0290), which is necessary for the LDCM software to function. Future BIOS will automatically disable the onboard LM78 if the ASMM is detected. You can manually disable the motherboard's LM78 if your BIOS does not have this feature. If your motherboard does not have LM78, no modifications are necessary to use the LDCM software.

Procedures for disabling the motherboard's LM78:

1. Create a bootable disk by formatting a floppy disk with system files.
2. Copy the PCI control program PCICFG.EXE to the disk
3. Copy the DOS utility DEBUG.COM to the disk (NOTE: DEBUG.COM must be the same version as the DOS version on the disk otherwise, it will not run)
4. With the disk inserted, restart the system and press DELETE to enter BIOS setup.
5. Adjust the BIOS boot sequence to *A:, C:* (that is, boot from floppy first).
6. Save and exit the BIOS setup.

   NOTE: Ignore the next hardware monitor error from the LM78 conflict.
7. Under the appropriate prompt signs, type the following:

A>	**PCICFG** <ENTER>
BUS00>	**WD 1 3 60 00670290** <ENTER> (disables the motherboard's LM78)
BUS00>	**Q** <ENTER> (exits the PCI control program)
A>	**DEBUG** <ENTER>
>	**A** <ENTER>
xxxx:0100	**int 19** <ENTER>
xxxx:01yy	<ENTER> (then remove the disk from the floppy drive)
>	**G** <ENTER>

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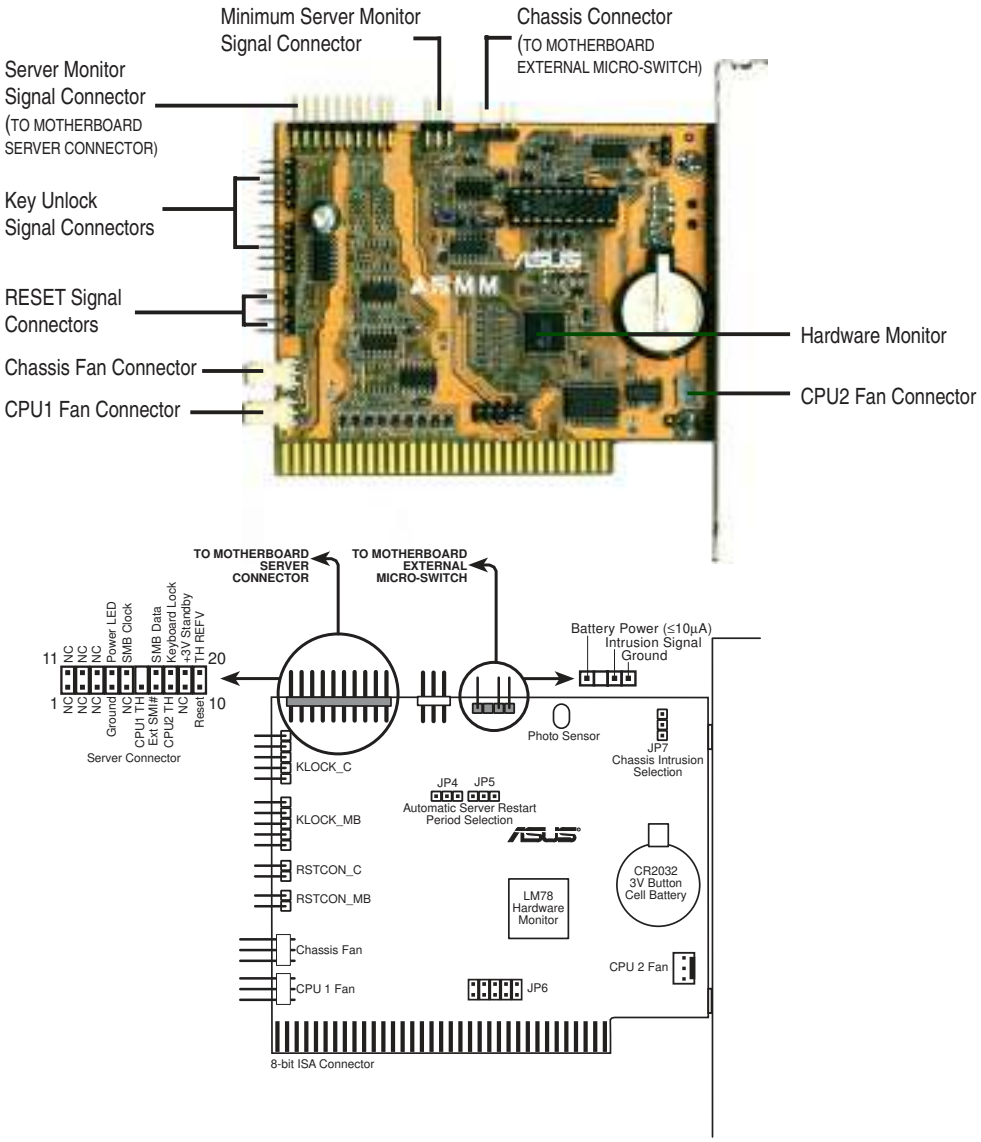
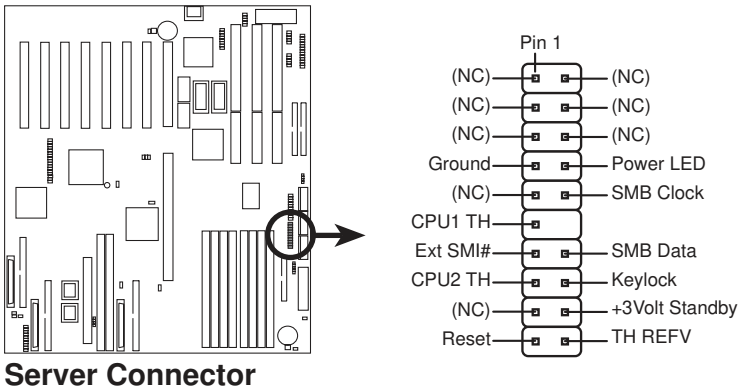
ASUS ASMM System Monitoring Module



Motherboard Server Connector



Server Connector

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Server Monitor Card Specifications

BUS: 8-bit ISA bus

Battery: Lithium battery, 210mA/hour

Thermal Monitoring: Onboard temperature sensor

Voltage Monitoring: +12V, -12V, +5V, -5V, +3.3V (+3.3V needs external cable)

Fan Speed Monitoring: 3 tachometers are provided to detect fan speed as low as 660rpm(needs cooling fan with extra signal line)

Chassis Intrusion Monitoring: Optical chassis detection circuit is built-in (external intrusion detection connector is also provided)

Security Mode: Keyboard lock/unlock, Reset enable/disable (requires Feature cable)

Automatic Server Reset/Restart: Server can be hard reset after a system hang is detected (requires Feature cable)

Mechanical: Half-length ISA card (length: 10.3cm, height: 8.8cm)

Connectors
20-pin external Feature connector for ASUSTeK SMH (Server Monitor Header)
5-pin external keylock connector
2-pin external reset connector
5-pin keylock panel connector
2-pin reset panel connector
3-pin extended fan connectors

System Monitor

Voltages: +5V, -5V, +12V, -12V, +3V

Temperature: Card temperature

Tachometer: 3 fan speed detectors

Chassis Intrusion: Onboard Photo-resistor and Chassis intrusion external connector

ASR Reset Status: Under ASR (Automatic Server Restart) Test mode, one can access the status of ASR RESET signal while no real system reset will be active.

Card Rev. ID: For future upgradability, a card rev. ID is provided to enable the software to identify the card and adapt for it.

ASR Status: One can recognize whether the ASR function is enabled or disabled.

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System Control

Reset Button: Hard reset enable/disable

Keylock: keyboard lock/unlock

ASR: Enable, disable, and test

ASR period: ASR period selection through mini-jumper (30/120/240/330 seconds)

Chassis Intrusion: As this status will be backup through battery, one can clear the memorization of intrusion circuit.

System Notification

The system can be notified when the voltage/temperature/fan speed exceeds the predefined thresholds. The notification mechanism can be as simple as polling or through SMI#/IRQ service routine, depending on the programming of LM78. Five ISA IRQs can be selected (IRQs 3, 4, 5, 6, 7) through hardware jumper.

ASMM Color-Coded Cabling

These connections are classified into 3 categories: chassis intrusion, fan monitor, and server monitor.

Chassis intrusion: Chassis intrusion permits the activation of a user-installed alarm. One 3-wire cable supports the external customized chassis intrusion alarm. The pin definitions are: RED (battery power), YELLOW (intrusion signal), and BLACK (ground). The external intrusion signal should be open-drained.

Fan monitor: The fan monitor provides power for up to 3 fans while monitoring the connected fans' rotation through the specially designed tachometer. Three 3-wire cables are used to extend the length of each fan connection. The pin definitions are: YELLOW (tachometer signal), RED (+12V), and BLACK (ground).

Server monitor: The server monitor contains many signals that can be monitored and controlled through the software. The server monitor signals are: CPU voltage ID for Pentium II processor (N.A. in P/I-P65UP8), key lock and reset, CPU1 and CPU2 Vcore (N.A. in P/I-P65UP8), +3.3V, I2C bus (N.A. in P/I-P65UP8), and CPU1 and CPU2 thermister (N.A. in ASMM), EXTSMI#. One 20-wire ribbon cable is used. The red stipe indicates pin 1.

NOTE: If you want to test the security mode, the KEYLOCK and RESET connections must be correct. If the position of the reset signal is wrong, the reset inhibit function may not work.

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Programming Interface

LM 78

The LM78 address is fixed on I/O port 0x0290–0x0297 by default, as follows:

0x0290	Power On Self Test codes from ISA bus
0x0294	Power On Self Test codes from ISA bus
0x0295	The LM78 internal Address register
0x0296	Data register

For the relative programming interface, refer to the N.S. LM78 data sheet.

Automatic Server Restart

Four I/O ports are defined in this revision and are allocated on I/O space 0x0298–0x029F by default. These 4 I/O ports are ASR status/control register, Chassis intrusion reset register, ASR trigger register, and ASR enable/disable register.

ASR Status/Control Register (0x0298/Read/Write)

Read (*default value:* 00x0001)

bit 7:6 Card revision ID

00	SMC rev 1.x
others	Reserved

bit 5 ASR under reset. Because ASR needs a much longer time to be reset, this bit should be polled by the BIOS/application before it can be accessed. A "0" indicates the ASR is under reset such that the BIOS/application must wait until it becomes a "1". A "1" means the ASR is now out of reset and free for access.

bit 4 ASR test output. Under test mode, a "0" indicates a timeout event occurred as being too long without writing to the ASR trigger register.

bit 3 ASR enable or disable. A "0" depicts ASR function is disabled; a "1" indicates the ASR is enabled. While ASR is enabled, if the ASR is not under test mode, ASR trigger register must be written within a pre-specified time period or the system will get a hard reset.

bit 2 Mode select A

"0" Secure mode is disabled (default)

"1" Secure mode is selected. The system will enter the secure mode (keyboard is locked, reset button is disabled) after a special I/O write sequence is executed.

bit 1 Mode select B

"1" ASR is in normal mode. The ASR can be enabled after a special I/O write sequence is executed.

"0" ASR is under test mode.

bit 0 System in secure mode. A "0" indicates the system is now under secure mode. A "1" depicts the system is now free for control.

Write

bit 7:3 Reserved.

bit 2 Mode select A

Writing a "1" will select secure mode while it will be enabled after a special I/O write sequence is executed. A "0" will deselect the secure function.

NOTE: If secure mode is selected and entered, deselecting the secure mode will not free the system out of secure mode. You must execute the special I/O write sequence to disable the secure function.

bit 1 Mode select B

Writing a "1" will select ASR under normal mode while ASR will be enabled after a special I/O write sequence is executed. A "0" will deselect the secure function.

bit 0 Reserved

NOTE: If ASR is enabled, putting ASR in test mode will not get the system out of the ASR normal mode. You must execute the special I/O write sequence to disable the ASR function.

Chassis Intrusion Reset Register (0x0299/Write only)

Writing any value to this I/O port will clear the memory of the chassis intrusion circuit. This function may only be activated under administrator control. The status of chassis intrusion can be retrieved by accessing LM78.

ASR Trigger Register (0x029A/Write only)

Periodically executing I/O write to this port will keep the system reset from driving. Otherwise, a system hard reset will be generated after a pre-specified period of time with no I/O write to this register if ASR is enabled.

ASR Enable/Disable Register (0x029B/Write only)

A data pattern of **xxxx_0001**b must be written into this port to produce a special I/O write sequence to enable ASR and secure function.

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ASR Enable/Disable Sequence and Test

The ASR function will be enabled by **consecutively writing** three I/O writes to the ASR enable/disable register with data pattern of xxxx_0001b. After these I/O writes are executed, bit 3 of the ASR status/control register will be set to "1" and bit 4 of the ASR status/control register will become "0" when there is no I/O write to the ASR trigger register within a pre-specified period of time. (The time period can be selected through 2 mini-jumpers with 30-, 90-, 240-, 330-second options.) The system will get a reset if the bit 1/Mode Select B of the ASR status/control register is set to "1" (normal mode). Otherwise, no system reset will be generated; the application can test the function of the ASR circuit by polling bit 4 of the ASR status/control register without writing to the ASR trigger register for the pre-specified time for checking whether it becomes "0" or not. If it is not, the ASR is malfunctioning. If it is, the application can then issue an I/O write to the ASR trigger register and wait for 30ms. Then bit 4 of the ASR status/control register can be checked again to see if it has changed to "1". If it has, the ASR circuit is correct. Otherwise, the ASR function is not working.

After the ASR function is enabled, **consecutively writing** three I/O writes to the ASR enable/disable register with data pattern "xxxx_0001" can disable the ASR function. It can be verified by reading bit 3 of the ASR status/control register to check if it has changed "0". If it has, the ASR is disabled. Otherwise, the SMC card is malfunctioning.

Secure Mode Enable/Disable Sequence

The system will enter secure mode only when bit 2/Mode Select A of the ASR status/control register is set to "1", then **two consecutive** I/O writes to the ASR enable/disable register with data pattern "xxxx_0001" and then **another consecutive** I/O write to the ASR trigger register are completed. While the system is under secure mode, the keyboard will be locked and reset button disabled.

Two consecutive I/O writes to the ASR enable/disable register with data pattern "xxxx_0001" and then **another consecutive** I/O write to ASR trigger register will bring the system out, unlock the keyboard and enable the reset button.

Early Access of ASR

Because the ASR needs more time to be reset (1 more second than the main system), unexpected problems can occur if someone tries to access/test/arm the ASR in the BIOS/application while the ASR is still under reset. So, a new status bit called "ASR under reset" has been added to the ASR status/control register so that the BIOS/application can poll this bit first to make sure the ASR is out of reset and free for access. Before you access the ASR, you must test this bit and check the related ASR setting (that is, the ASR setting is what you want it to be) as long as there is any possibility that the ASR has been reset for some other reason. For the BIOS, this bit must be tested before it can access/control the ASR.

Jumper and Connector Settings

Jumpers

JP1: LM78 I/O space select (Option**; PROVIDED BY NEGOTIATION**)

1-2 0x0290–0x0297 (default)
3-4 0x02B0–0x02B7
5-6 0x02D0–0x02D7
7-8 0x02F0–0x02F7

JP2: ASR I/O space select (Option**; PROVIDED BY NEGOTIATION**)

1-2 0x0398–0x039F
3-4 0x03B8–0x03BF
5-6 0x03D8–0x03DF
7-8 0x03F8–0x03FF

JP3: FAN 3 double pulse selection (Option**; PROVIDED BY NEGOTIATION**)

1-2 FAN 3 gets normal FAN pulse signal (default **SHORT**)
2-3 FAN 3 gets double FAN pulse signal

JP4/JP5: ASR period selection

JP4	JP5	Period select
2-3	2-3	5.5 min
1-2	2-3	4 in
2-3	1-2	1.5 min
1-2	1-2	30 sec

JP6: LM78 IRQ selection

JP6	IRQ select	JP6	IRQ select
1-2	IRQ3	7-8	IRQ6
3-4	IRQ4	9-10	IRQ7
5-6	IRQ5		

NOTE: Only one jumper can be set or IRQ lines will get conflict.

JP7: Chassis intrusion selection

JP7	Period select
2-3	Disable the Chassis intrusion detection on ASMM
1-2	Enable the Chassis intrusion detection on ASMM

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Connectors

• **SERVER_CON:** Full set server monitor signal connector

Pin#	Name	I/O	Description
1	VID4	I	Pentium II VID4
2	VID2	I	Pentium II VID2
3	VID0	I	Pentium II VID0
4	PGND	-	Power LED ground connect
5	VCORE 1	I	VCORE voltage from CPU 1
6	THRMR-R1	I	One thermister on motherboard (default for CPU1)
7	EXTSMI#	O	EXTSMI# to generate SMI# signal (O.D.)
8	THRMR-R2	I	The other thermister terminal on motherboard (default for CPU2)
9	THRM#	O	A signal to indicate abnormal temperature is detected (O.D.)
10	RESET#	O	RESET signal to hard reset motherboard (O.D.)
11	VID3	I	Pentium II VID3
12	VID1	I	Pentium II VID1
13	VCORE 2	I	VCORE voltage from CPU 2
14	PLED	-	Power LED power connect
15	SMBCLK	I	I2C bus clock (O.D.)
16	Key		
17	SMBDATA	I/O	I2C bus data (O.D.)
18	KEYUNLK	-/O	Key unlock signal for motherboard (O.D.)
19	+3V	I	+3V from motherboard for measurement
20	Vtherm	O	Reference voltage for thermister

• **MINI_CON:** Minimum server monitor signal connector

Pin#	Name	I/O	Description
1	THRMR-R1	I	One thermister terminal on motherboard
2	+3V	I	+3V from motherboard for measurement
3	THRM#	O	A signal to indicate abnormal temperature is detected (O.D.)
4	Vtherm	O	Reference voltage for thermister
5	Key		
6	VCORE	I	VCORE voltage from CPU

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- **KLOCK_A/KLOCK_B**: Key unlock signal connectors for intercepting the KEYUNLK signal for processing.

Pin#	Name	I/O	Description
1	Power LED	-	+5V for Power LED
2	N.C.		
3	GND	-	GROUND
4	KEYUNLK	-	KEY unlock signal
5	GND	-	GROUND

NOTE: The key unlock connector from the chassis can be connected to either one of these connector while the other connector must be connected to the motherboard key unlock header

- **RSTCON_A/RSTCON_B:** RESET signal connectors to intercept the reset button for processing

The reset signal connector from the chassis can be connected to either one of these connector while the other connector must be connected to the motherboard reset button header.

- **EXT_I2C:** External I2C bus connector to provide external access to the system resource from the I2C bus.

Pin#	Name	I/O	Description
1	SMBDATA	I/O	I2C bus data (O.D.)
2	+5V	O	Power for external I2C device
3	GND	-	GROUND
4	SMBCLK	I	I2C bus clock (O.D.)

- **CHASSIS:** Header designed to provide a connection to the customer's self-designed chassis intrusion hardware.

NOTE: Because the hardware is powered by battery, the power consumption must be carefully limited. It is 20 µA for the external detection circuit.

Pin#	Name	I/O	Description
1	BATT	-	+3V power for external circuit
2	INTRUD	I	Chassis intrusion signal. "H" indicates intrusion. "L" indicates chassis is closed. **H:** above or equal to 2.5V; **L:** below or equal to 0.8V
3	GND	-	GROUND